IN THE SPECIFICATION

Please amend the paragraph at page 4, lines 2-6, as follows:

a first semiconductor layer of non-doped $A1_XGa_{1-X}N$ ~~(0 = X = 1)~~ (0 ≤ X ≤ 1);

a second semiconductor layer of non-doped or n-type $A1_YGa_{1-Y}N$ ~~(0 = Y = 1, X < Y)~~ (0 ≤ Y ≤ 1, X < Y)

disposed on the first semiconductor layer;

Please amend the paragraph at page 4, lines 23-27, as follows:

a first semiconductor layer of non-doped $A1_XGa_{1-X}N$ ~~(0 = X = 1)~~ (0 ≤ X ≤ 1);

a second semiconductor layer of non-doped or n-type $A1_YGa_{1-Y}N$ ~~(0 = Y = 1, X < Y)~~ (0 ≤ Y ≤ 1, X < Y) disposed on the first semiconductor layer;

Please amend the paragraph at page 5, lines 1-5, as follows:

first and second contact layers of n-type $A1_ZGa_{1-Z}N$ ~~(0 = Z = 1)~~ (0 ≤ Z ≤ 1)

disposed separately from each other on or in a surface of the second semiconductor layer, and having a resistivity lower than that of the second semiconductor layer;

Please amend the paragraph at page 5, lines 21-25, as follows:

a first semiconductor layer of non-doped $A1_XGa_{1-X}N$ ~~(0 = X = 1)~~ (0 ≤ X ≤ 1);

a second semiconductor layer of non-doped or n-type $A1_YGa_{1-Y}N$ ~~(0 = Y = 1, X < Y)~~ (0 ≤ Y ≤ 1, X < Y) disposed on the first semiconductor layer;

Please amend the paragraph beginning at page 10, line 27, ending at page 11, line 8, as follows:

As shown in FIG. 1, this power HEMT includes a channel layer (first semiconductor layer) 1 of the non-doped type disposed on a support substrate S1 of sapphire, and a barrier layer (second semiconductor layer) 2 of the non-doped or n-type disposed on the channel layer 1. The channel layer 1 consists of $Al_XGa_{1-X}N$ ~~$(0=X=1)$~~ $(0 \leq X \leq 1)$, e.g., GaN. The barrier layer 2 consists of $Al_YGa_{1-Y}N$ ~~$(0=Y=1, X<Y)$~~ $(0 \leq Y \leq 1, X < Y)$, e.g., $Al_{0.2}Ga_{0.8}N$.

Please amend the paragraph beginning at page 19, line 20, ending at page 20, line 5, as follows:

The channel layer 31 consists of $Al_XGa_{1-X}N$ ~~$(0=X=1)$~~ $(0 \leq X \leq 1)$, e.g., GaN. The barrier layer 32 consists of $Al_YGa_{1-Y}N$ ~~$(0=Y=1, X<Y)$~~ $(0 \leq Y \leq 1, X < Y)$, e.g., $Al_{0.2}Ga_{0.8}N$. On the other hand, the source and drain contact layers 33 and 34 may be formed of a process that forms a groove by etching and then forms a buried layer therein by selective growth; a process that employs ion implantation of an n-type impurity and heat treatment; or the like. Accordingly, the compositions of the source and drain contact layers 33 and 34 are determined by the process. However, the source and drain contact layers 33 and 34 can be expressed by a general formula, $Al_ZGa_{1-Z}N$ ~~$(0=Z=1)$~~ $(0 \leq Z \leq 1)$.

Please amend the paragraph at page 23, lines 9-23, as follows:

As shown in FIG. 7, this power HEMT includes semiconductor layers 31 and 32, electrodes 43, 44, 45, 47, and 48, and an insulating film 46 in the same manner as in the power HEMT shown in FIG. 6, while it includes source and drain contact layers 33X and 34X disposed in a different manner from the source and drain contact layers 33 and 34 shown in FIG. 6. The source and drain contact layers 33X and 34X consist of a semiconductor layer that is formed by crystal growth and patterning on the barrier layer 32, and expressed by a

general formula, $Al_ZGa_{1-Z}N$ ~~$(0 = Z = 1)$~~ $(0 \leq Z \leq 1)$. The source and drain contact layers 33X and 34X protrude on the surface of the barrier layer 32, and a gate electrode 33 is interposed therebetween. Namely, this device structure is of the recess gate type.

Please amend the paragraph at page 24, lines 10-17, as follows:

As shown in FIG. 8, this power HEMT includes a lower layer 36 of the p-type disposed below a channel layer 31, in addition to the same device structure as the power HEMT shown in FIG. 6. The lower layer 36 consists of $Al_XGa_{1-X}N$ ~~$(0 = X = 1)$~~ $(0 \leq X \leq 1)$, e.g., GaN. The lower layer 36 is electrically connected to a source electrode 44 through an electrode and interconnection L3.

Please amend the Abstract at page 39, lines 1-17, as follows: